Cu Electroless Bottom-up Filling Techniques for ULSI Interconnect Fabrication

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Electroless deposition technology is expected to be widely used for ultra large scale integration (ULSI) interconnects due to its low process cost and temperature as well as excellent step coverage and selectivity. In particular copper (Cu) electroless deposition has a high potential in the application to both the repairing process for defects of physical vapor deposition (PVD) seed occurring as the feature size shrinks and the seed layer formation for electrodeposition. Currently, defect-free Cu filling using only electroless deposition in vias or trenches without sequential electrodeposition is being studied. In this article, the effect of bis-(3-sulfopropyl)-disulfide (SPS), a well-known additive for bottom-up filling in Cu electrodeposition was investigated in Cu electroless deposition. Additionally, studies on the co-addition of surfactant with SPS and another additive for bottom-up filling were performed to improve the property and quality of electrolessly gap-filled Cu.