Lead-Lag Compensators Design for Higher Order SISO Dead-Time System Regulatory Control

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A simplified algorithm for designing a lead-lag compensator for higher order SISO dead-time regulatory control system is proposed in this paper. The lead-lag compensator is designed in order to satisfy the control specifications in time domain such as damping ratio, maximum overshoot settling time and steady state error. Using the correlation between frequency and time domain, the algorithm can also be used to solve the required compensator in the case the design specifications are given in frequency domain, such as phase margin and gain margin. The proposed lead-lag compensator design technique directly satisfies time domain control specifications such as damping ratio, maximum overshoot, settling time and steady state error without trial and error steps. This study was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2015R1D1A3A01015621) and by Priority Research Centers Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2014R1A6A1031189).