Effects of Surface Energy and Roughness of Gate Dielectrics on OFET Characteristics

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The effects of surface energy of polymer gate dielectrics on pentacene morphology and the electrical properties of pentacene based field effect transistors (FETs) are reported using surface energy controllable poly(imide-siloxane)s as gate dielectric layers. The surface energy of gate dielectrics strongly influences the pentacene film morphology and growth mode, producing layer-by-layer growth with large and dendritic grains at high surface energy and 3D island growth with small grains at low surface energy. The surface roughness is also important factor. Roughened site may act as carrier trap during charge transport in organic semiconductor layer and also inhibits the uniform growth and the formation of large crystal grains. The morphology of pentacene depending on the roughness of gate dielectrics was analyzed using the dual layer structure gate dielectrics composed of spin-coated PMMA layer on the anodized Al_2O_3 layer. The rms roughness was controlled from 0.4 nm to 3 nm by adjusting the thickness of spin-coated PMMA layer. As the results of XRD and NEXAFS analyses, the layered structure of pentacene was disturbed by the roughness of dielectrics. However, the in-plane ordering which constitutes the co-facial structure of pentacene molecules was not affected by the roughness of dielectrics.