A hierarchical approach for fab-wide scheduling of the Intel mini-fab benchmark model

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A fab-wide scheduling in a semiconductor fabrication facility is challenging since the system has complex product flows including reentrant loops. The Intel mini-fab benchmark model which consists of one-product, six-step and five-machine manufacturing line captures challenges in scheduling reentrant manufacturing line such as disparate processing rates and batching. In this study, a two-layer hierarchical approach is developed for planning and scheduling of this model. At the bottom layer, a model predictive control (MPC) method based on an aggregated flow model is used to determine processing schedules per shift for each station. This layer allows the scheduler to simultaneously solve the constraint-aware production optimization and in-process inventory control problems at each scheduling instance. At the top layer, a scenario planning for addressing supply-side uncertainties (e.g., unpredictable equipment downtime) determines target work-in-process (WIP) levels that allow the fab to meet the expected demand without productivity loss or excessive cycle time.