Charge-up simulation coupled with unified semi-global surface model for UHARC plasma etching in semiconductor fabrication

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Current plasma etching technology faces a great challenge with the advent of next generation electronic devices such as 3D memory and FINFET in semiconductor industry. Especially, charge-up issues under plasma etching are recognized as bottleneck of forming the ideal etch profile because these effects can cause abnormal behavior of the ion transport inside nanoscale feature profile. To address these issues in this work, we developed a realistic surface reaction model of SiO2 plasma etching, and applied it to the charge-up simulation using 3D topography simulator named as K-SPEED. In our surface reaction model, the plasma etch under existence of the steady state passivation layer was considered with both a semi-analytical model of passivation layer and detailed kinetic models of plasma deposition and etching. Meanwhile, charge-up simulation was composed of ion transport module and 3D poisson equation. Finally, the realistic surface reaction model was incorporated into the 3D charge-up simulation in order to elucidate the unveiled physicochemical behavior under plasma etching of nanoscale feature.